FIG. 1

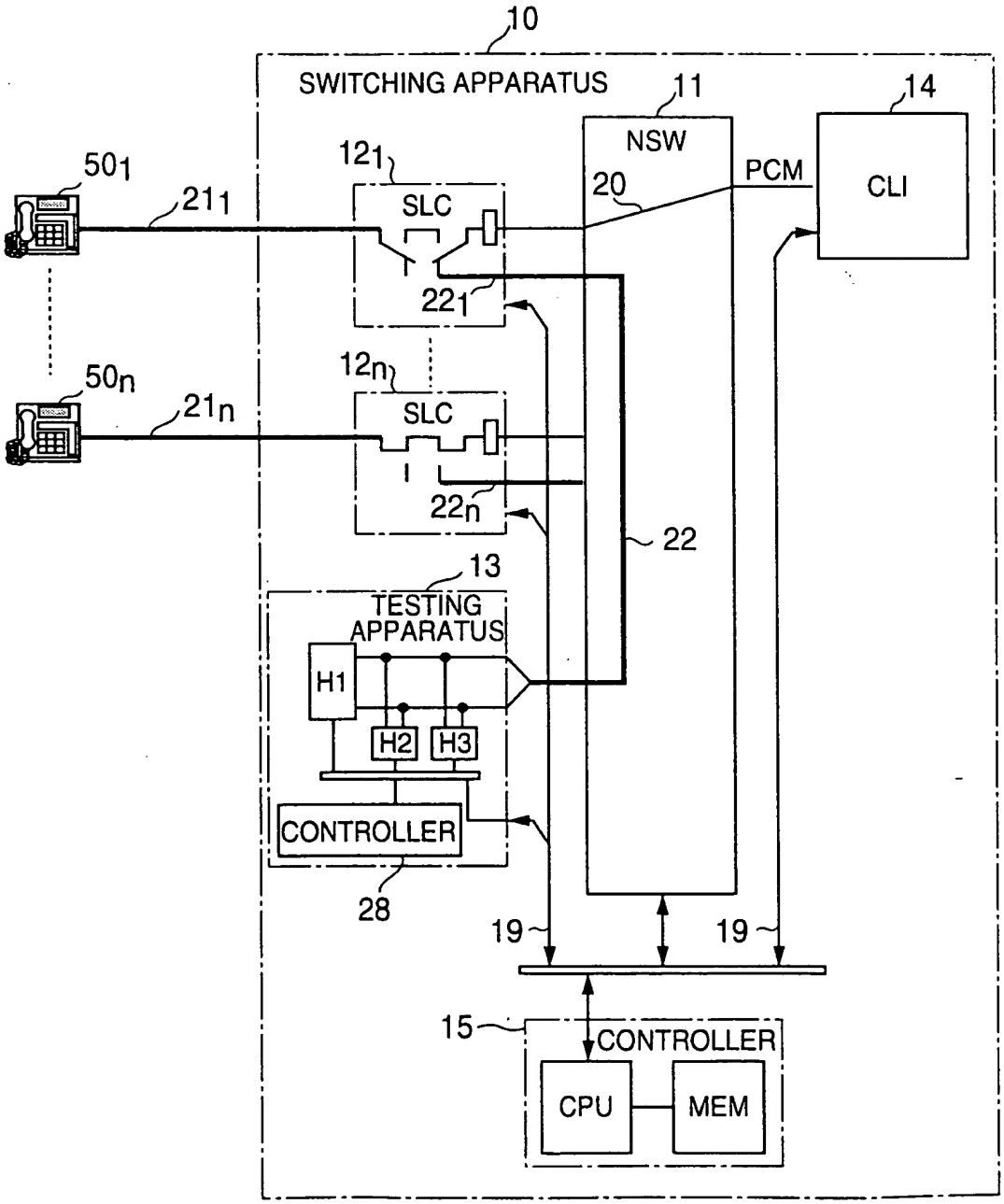

10
SWITCHING APPARATUS
11
NSW
14
CLI
PCM
20
121
SLC
501
211
221
12n
SLC
50n
21n
22n
22
13
TESTING APPARATUS
H1
H2
H3
CONTROLLER
28
19
19
15
CONTROLLER
CPU
MEM

FIG. 2

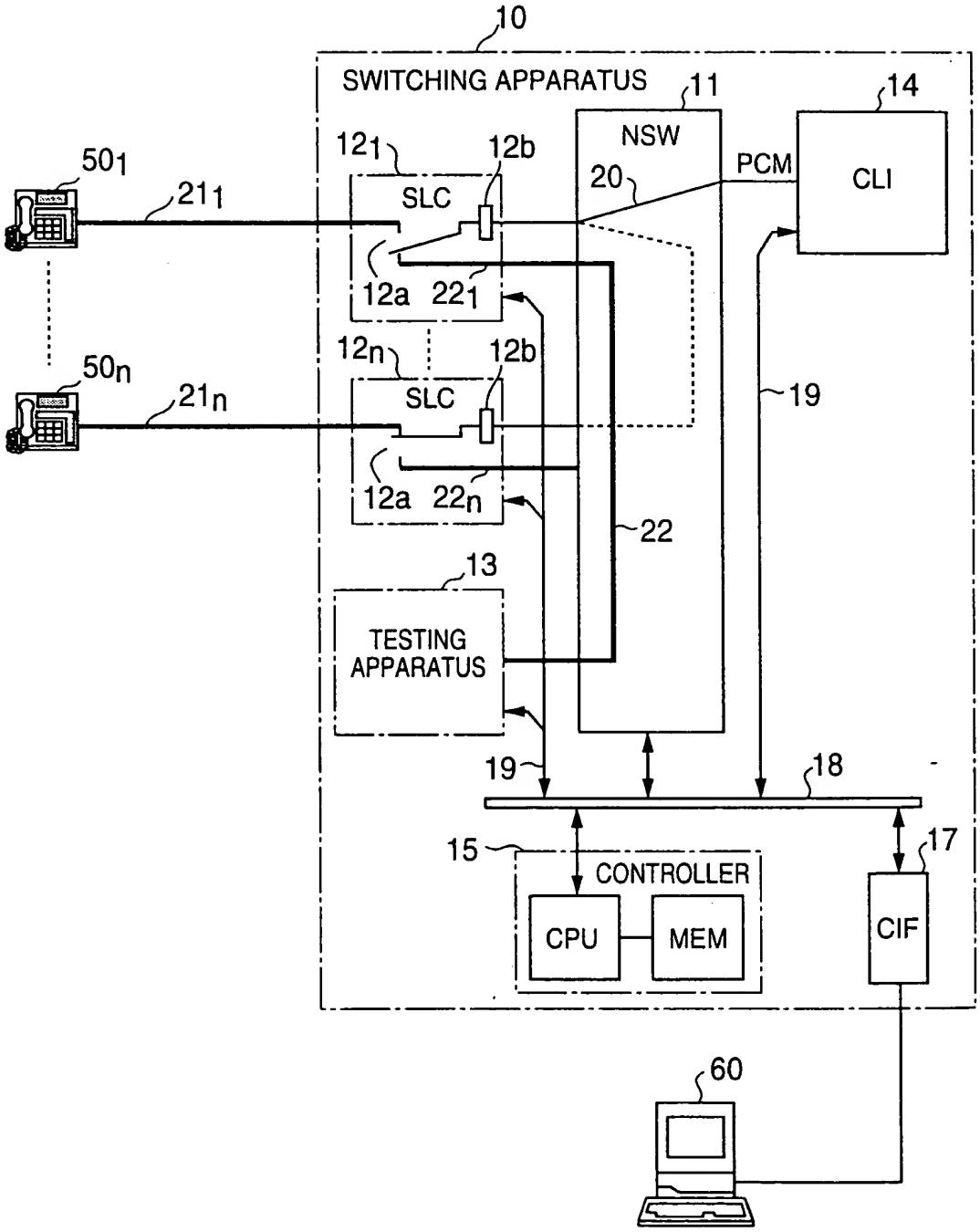

10
SWITCHING APPARATUS
11
NSW
14
CLI
PCM
20
121
12b
SLC
501
211
12a
221
12n
50n
21n
22n
19
22
13
TESTING APPARATUS
18
15
CONTROLLER
CPU
MEM
17
CIF
60

FIG. 3

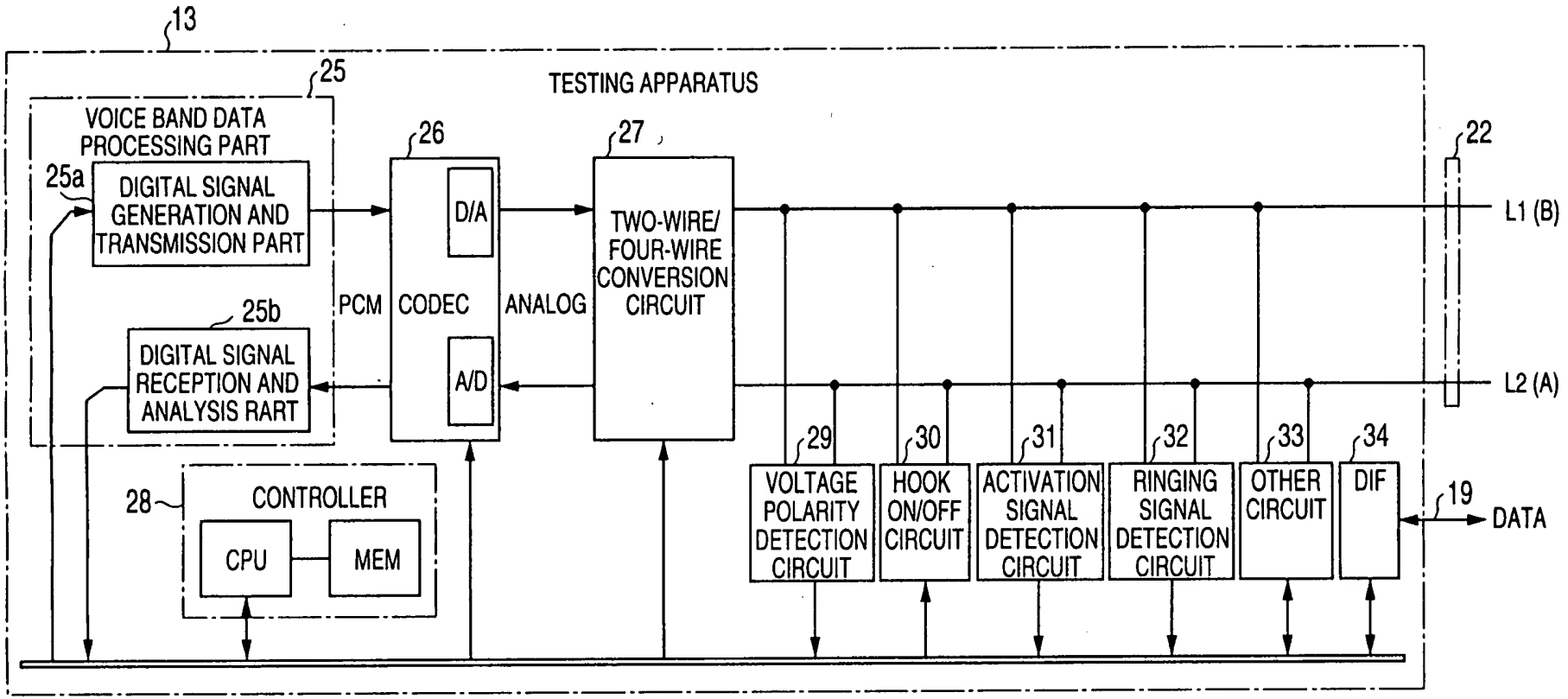

13
TESTING APPARATUS
25
VOICE BAND DATA PROCESSING PART
25a
DIGITAL SIGNAL GENERATION AND TRANSMISSION PART
25b
DIGITAL SIGNAL RECEPTION AND ANALYSIS RART
PCM
26
CODEC
D/A
A/D
ANALOG
27
TWO-WIRE/ FOUR-WIRE CONVERSION CIRCUIT
22
L1 (B)
L2 (A)
28
CONTROLLER
CPU
MEM
29
VOLTAGE POLARITY DETECTION CIRCUIT
30
HOOK ON/OFF CIRCUIT
31
ACTIVATION SIGNAL DETECTION CIRCUIT
32
RINGING SIGNAL DETECTION CIRCUIT
33
OTHER CIRCUIT
34
DIF
19
DATA

FIG. 4

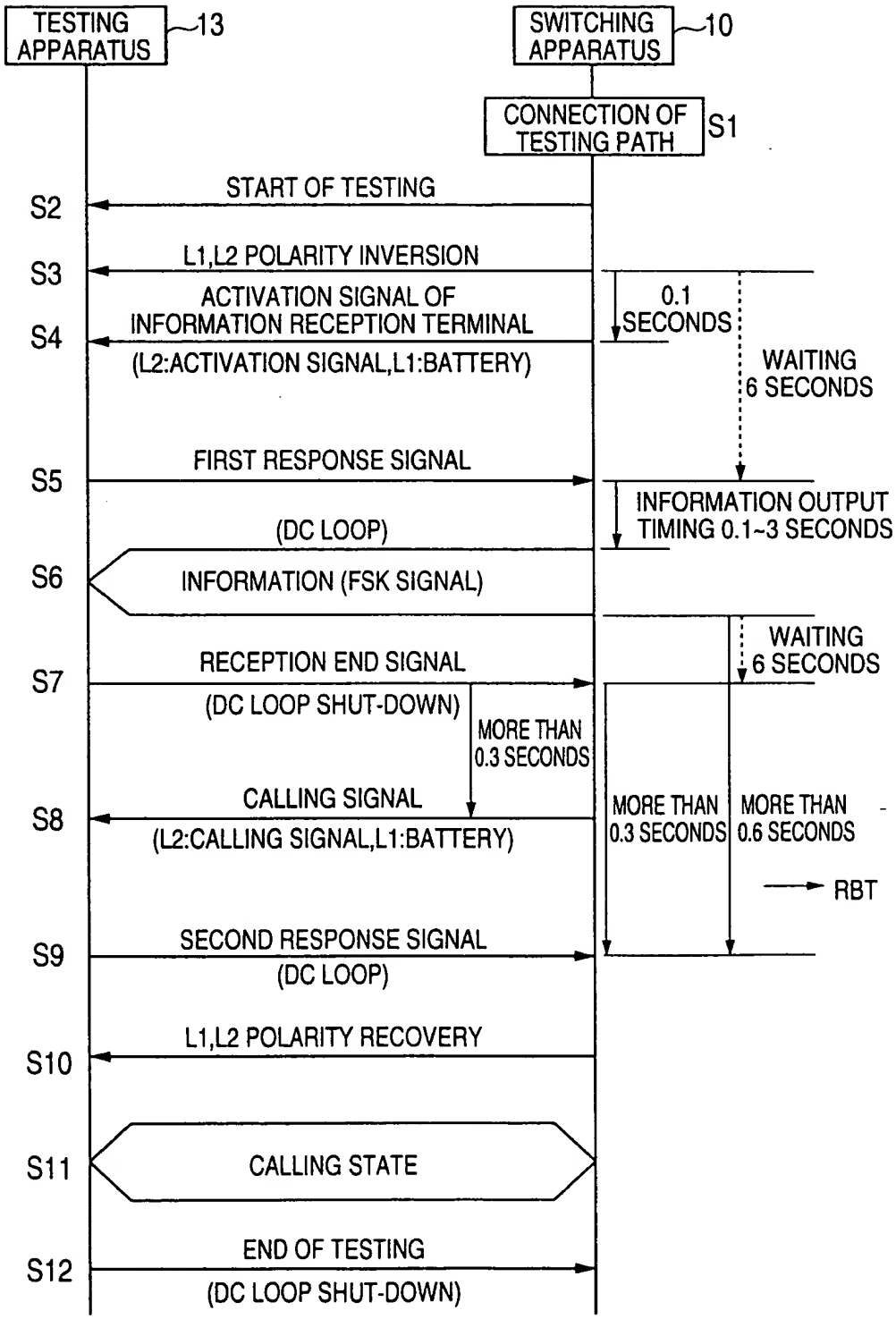

TESTING APPARATUS
13
SWITCHING APPARATUS
10
CONNECTION OF TESTING PATH
S1
START OF TESTING
S2
L1,L2 POLARITY INVERSION
S3
ACTIVATION SIGNAL OF INFORMATION RECEPTION TERMINAL
S4
(L2:ACTIVATION SIGNAL,L1:BATTERY)
0.1 SECONDS
WAITING 6 SECONDS
FIRST RESPONSE SIGNAL
S5
(DC LOOP)
INFORMATION OUTPUT TIMING 0.1~3 SECONDS
INFORMATION (FSK SIGNAL)
S6
WAITING 6 SECONDS
RECEPTION END SIGNAL
S7
(DC LOOP SHUT-DOWN)
MORE THAN 0.3 SECONDS
CALLING SIGNAL
S8
(L2:CALLING SIGNAL,L1:BATTERY)
MORE THAN 0.3 SECONDS
MORE THAN 0.6 SECONDS
RBT
SECOND RESPONSE SIGNAL
S9
(DC LOOP)
L1,L2 POLARITY RECOVERY
S10
CALLING STATE
S11
END OF TESTING
S12
(DC LOOP SHUT-DOWN)

FIG. 5

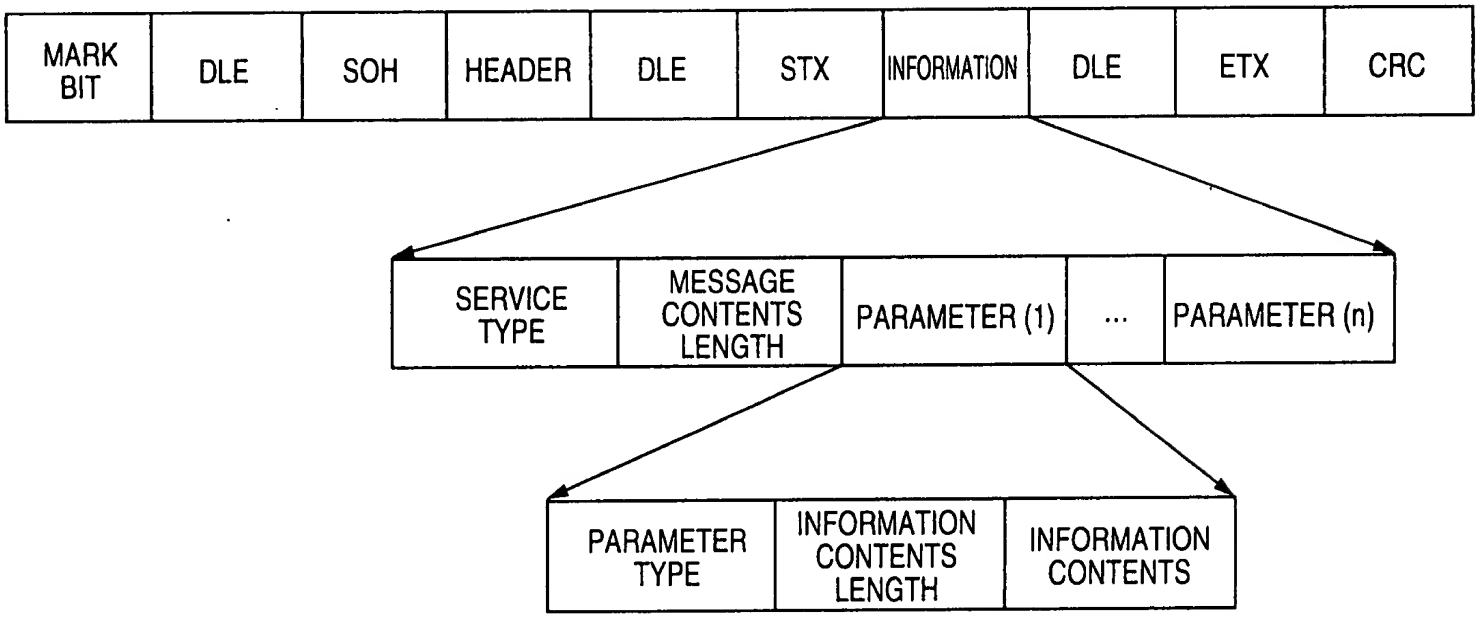
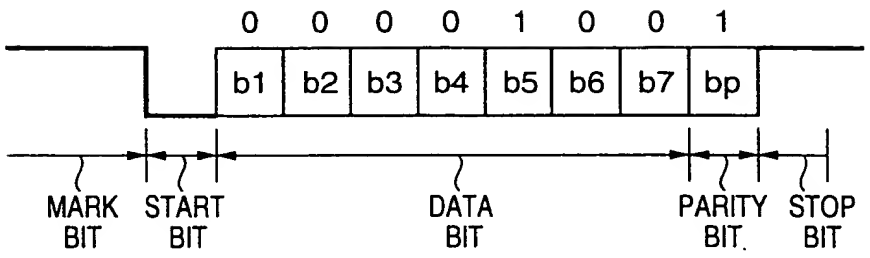

MARK BIT
DLE
SOH
HEADER
DLE
STX
INFORMATION
DLE
ETX
CRC
SERVICE TYPE
MESSAGE CONTENTS LENGTH
PARAMETER (1)
...
PARAMETER (n)
PARAMETER TYPE
INFORMATION CONTENTS LENGTH
INFORMATION CONTENTS

FIG. 6

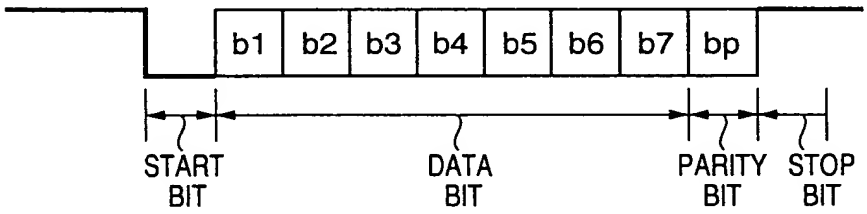
SIGNAL NAME	BIT REPRESENTATION	REMARKS
MARK BIT	SEQUENCE OF ONE	MORE THAN 60ms
CONTROL SIGNAL	B7~B1	FUNCTIONS
DLE	0010000	CONTROL SIGNAL FOR TRANSPARENT MODE
SOH	0000001	START OF HEADING OF INFORMATION
HEADER	0000111	SENDING INFORMATION FROM SWITCHING APPARATUS TO TERMINAL (BIN)
STX	0000010	START OF TEXT AND END OF HEADING
SERVICE TYPE	1000000	INFORMATION NOTIFICATION SERVICE BEFORE COMMUNICATION
MESSAGE CONTENTS LENGTH	0000001~1110101	TOTAL BYTES OF PARAMETER (1)~(n) (BIN)
PARAMETER TYPE		(BIN)
INFORMATION CONTENTS LENGTH		BYTE NUMBER OF PARAMETER (BIN)
INFORMATION CONTENTS		(CHARACTER PRESENTATION)
FTX	0000011	END OF TEXT
SI	0001111	USE OF ROMAN ALPHABET FOR FIGURE
SO	0001110	USE OF KATAKANA FOR FIGURE
CRC		16 BIT CRC RESULT

EP 0 560 254 A2

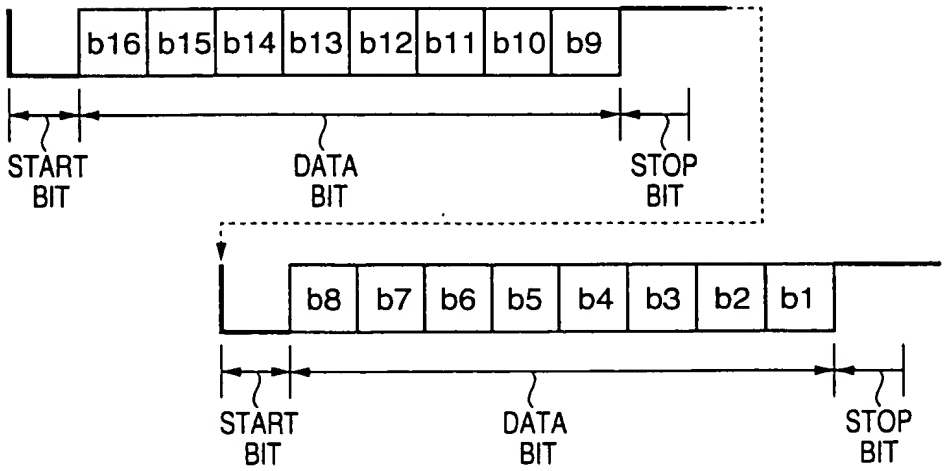
FIG. 7


0 0 0 0 1 0 0 1
b1 b2 b3 b4 b5 b6 b7 bp
MARK BIT
START BIT
DATA BIT
PARITY BIT
STOP BIT

(A)


b1 b2 b3 b4 b5 b6 b7 bp
START BIT
DATA BIT
PARITY BIT
STOP BIT

(B)


b16 b15 b14 b13 b12 b11 b10 b9
START BIT
DATA BIT
STOP BIT
b8 b7 b6 b5 b4 b3 b2 b1
START BIT
DATA BIT
STOP BIT

(C)

FIG. 8

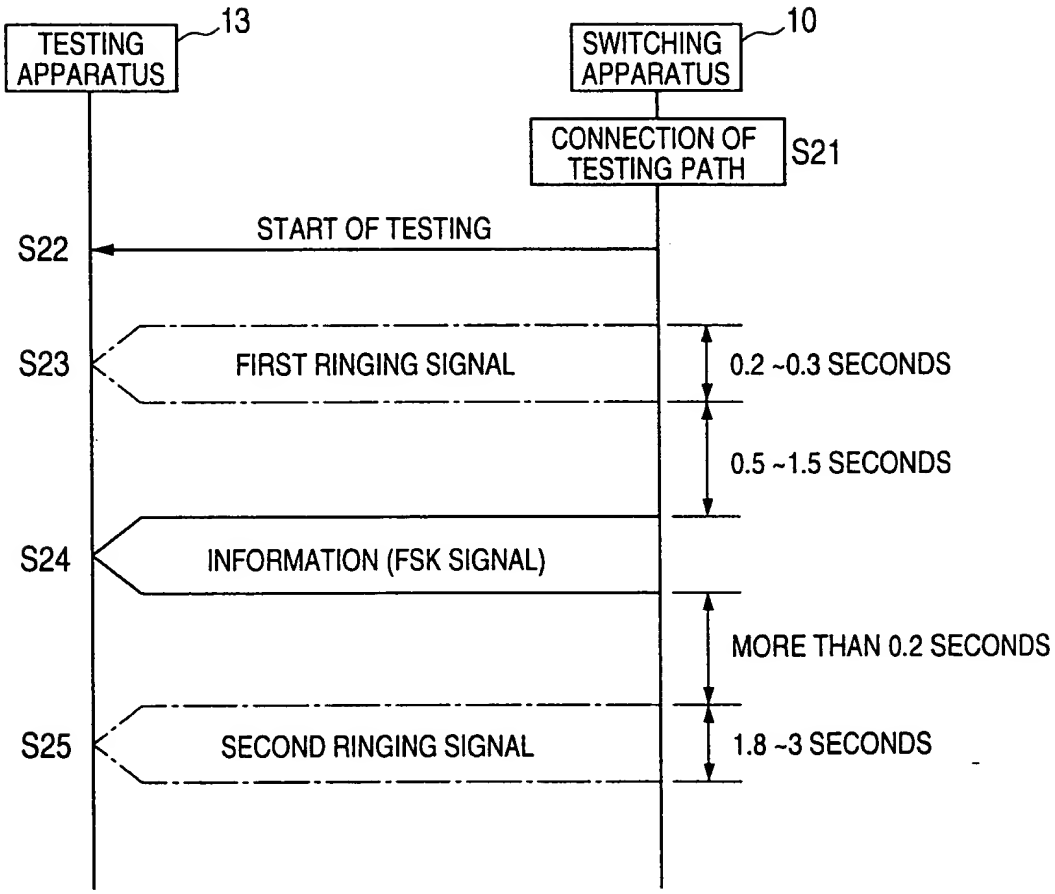
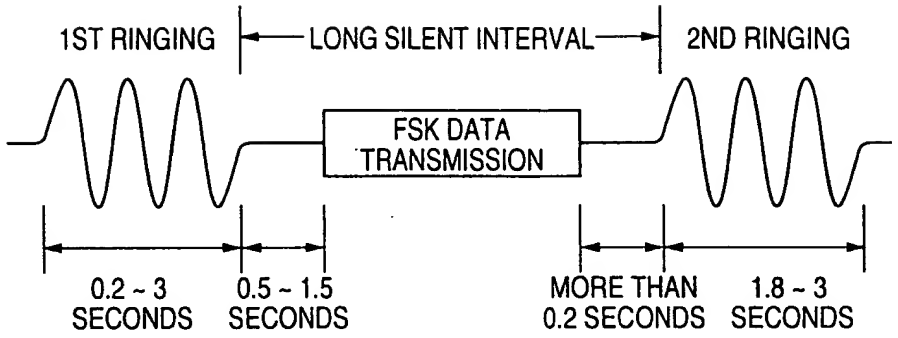
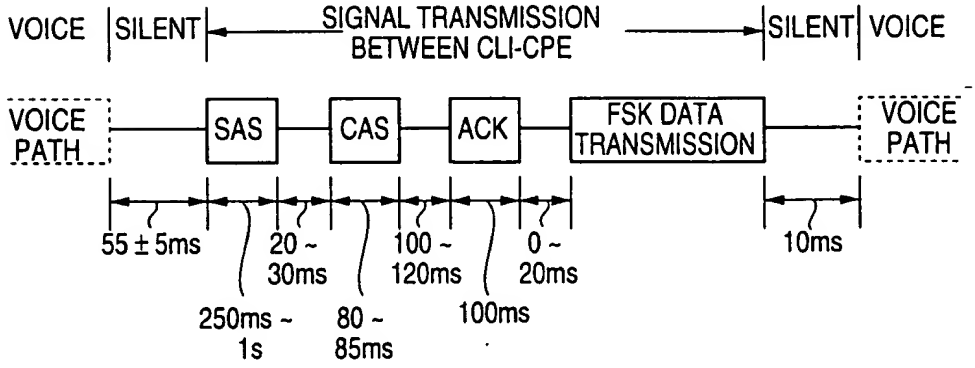

TESTING APPARATUS
13
SWITCHING APPARATUS
10
CONNECTION OF TESTING PATH
S21
START OF TESTING
S22
S23
FIRST RINGING SIGNAL
0.2 ~0.3 SECONDS
0.5 ~1.5 SECONDS
S24
INFORMATION (FSK SIGNAL)
MORE THAN 0.2 SECONDS
S25
SECOND RINGING SIGNAL
1.8 ~3 SECONDS

FIG. 9



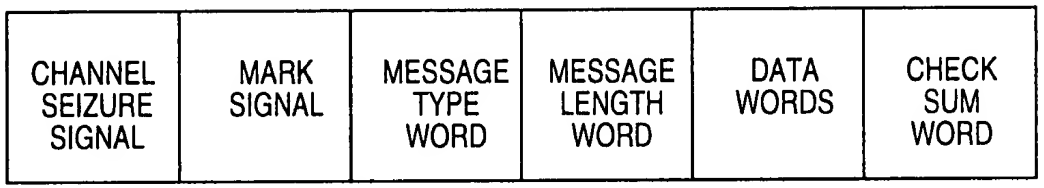
(A) ON-HOOK



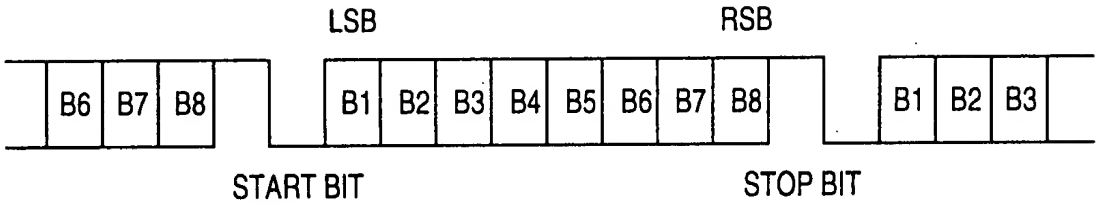
(B) OFF-HOOK

005007 8266960

FIG. 10



(A)



(B)

FIG. 11

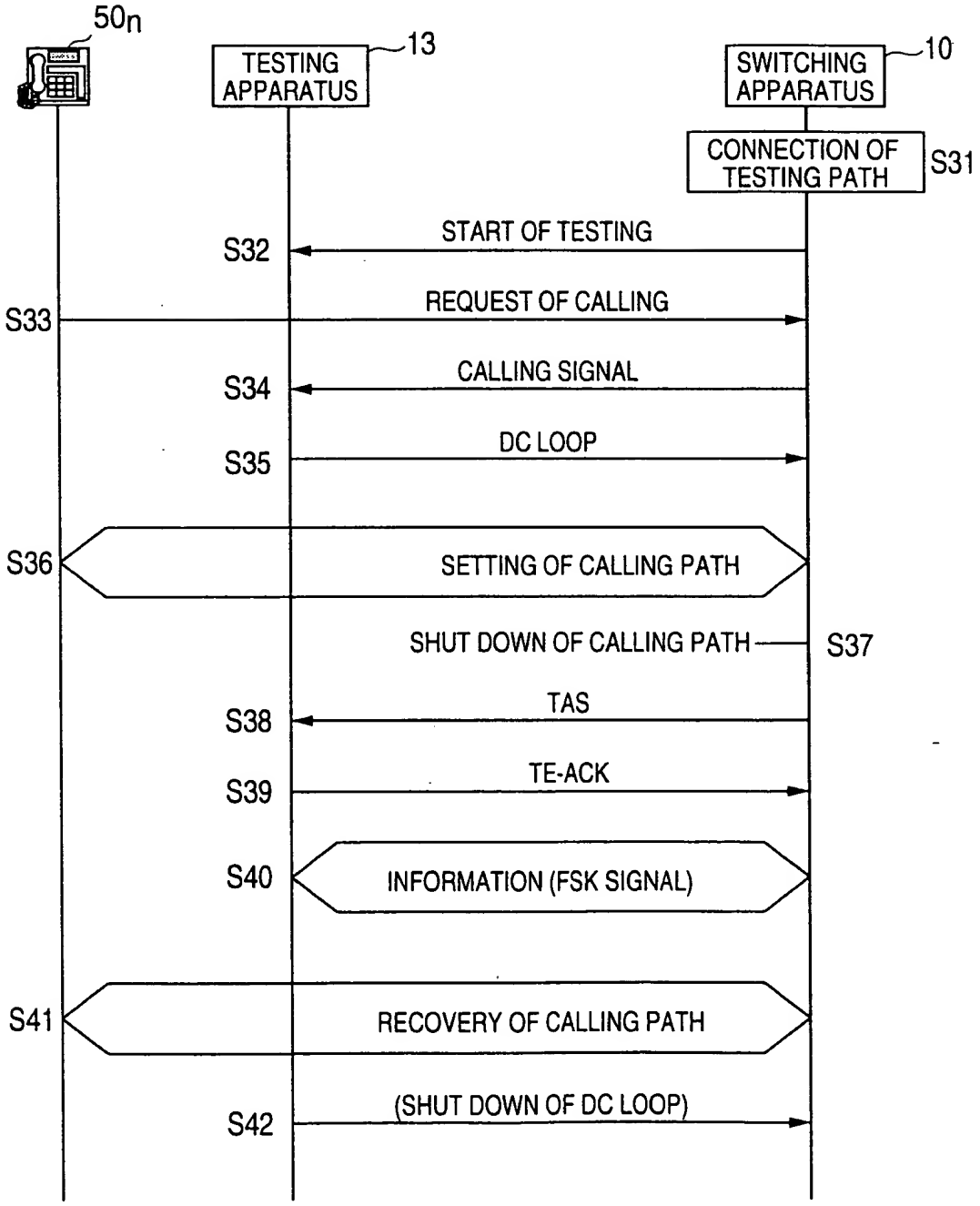

50n
TESTING APPARATUS
13
SWITCHING APPARATUS
10
CONNECTION OF TESTING PATH
S31
START OF TESTING
S32
REQUEST OF CALLING
S33
CALLING SIGNAL
S34
DC LOOP
S35
S36
SETTING OF CALLING PATH
SHUT DOWN OF CALLING PATH
S37
TAS
S38
TE-ACK
S39
S40
INFORMATION (FSK SIGNAL)
S41
RECOVERY OF CALLING PATH
(SHUT DOWN OF DC LOOP)
S42

FIG. 12

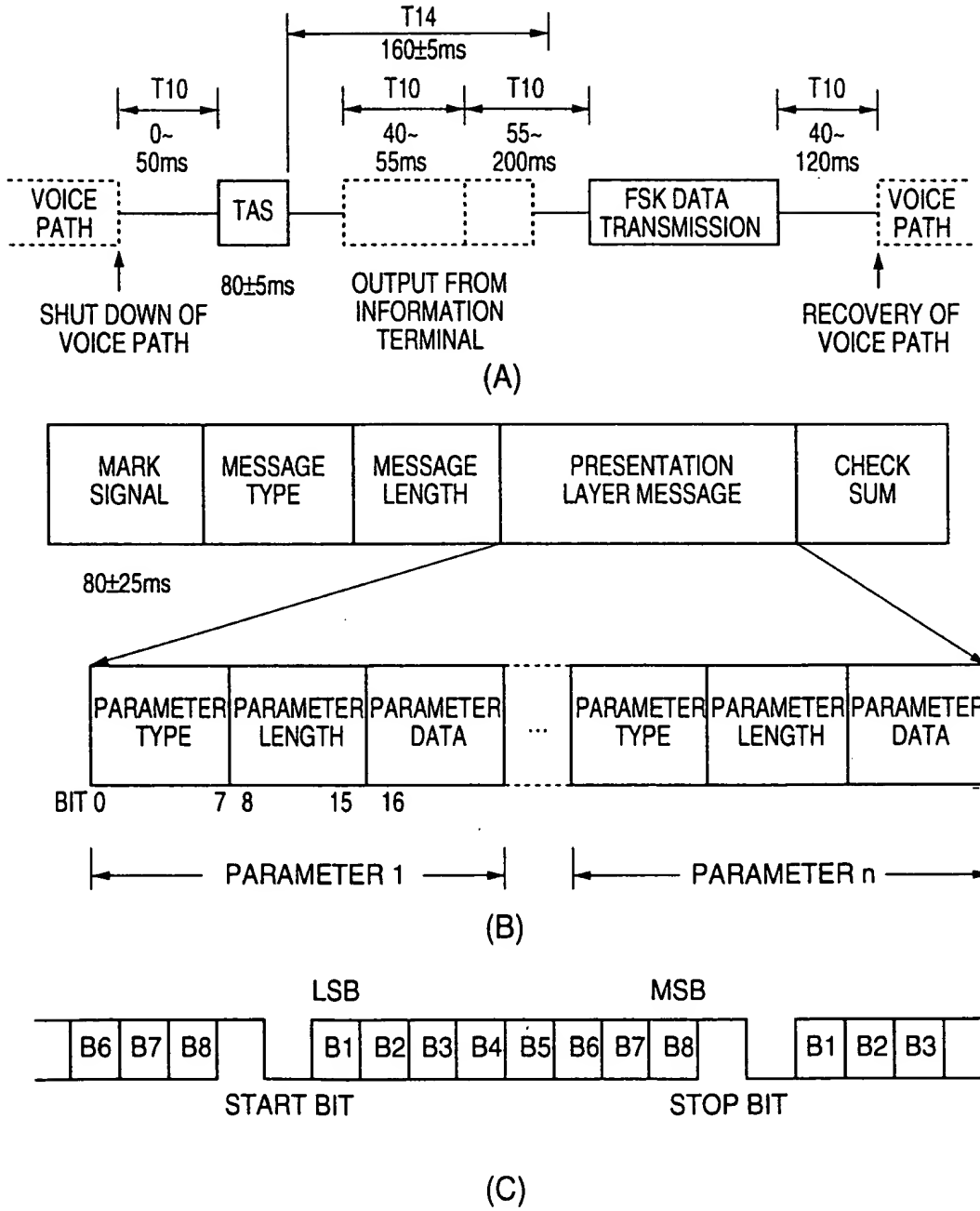

T14
160±5ms
T10
0~
50ms
T10
40~
55ms
T10
55~
200ms
T10
40~
120ms
VOICE PATH
TAS
FSK DATA TRANSMISSION
VOICE PATH
SHUT DOWN OF VOICE PATH
80±5ms
OUTPUT FROM INFORMATION TERMINAL
RECOVERY OF VOICE PATH
(A)
MARK SIGNAL
MESSAGE TYPE
MESSAGE LENGTH
PRESENTATION LAYER MESSAGE
CHECK SUM
80±25ms
PARAMETER TYPE
PARAMETER LENGTH
PARAMETER DATA
...
PARAMETER TYPE
PARAMETER LENGTH
PARAMETER DATA
BIT 0
7 8
15 16
PARAMETER 1
PARAMETER n
(B)
LSB
MSB
B6 B7 B8
B1 B2 B3 B4 B5 B6 B7 B8
B1 B2 B3
START BIT
STOP BIT
(C)

FIG. 13

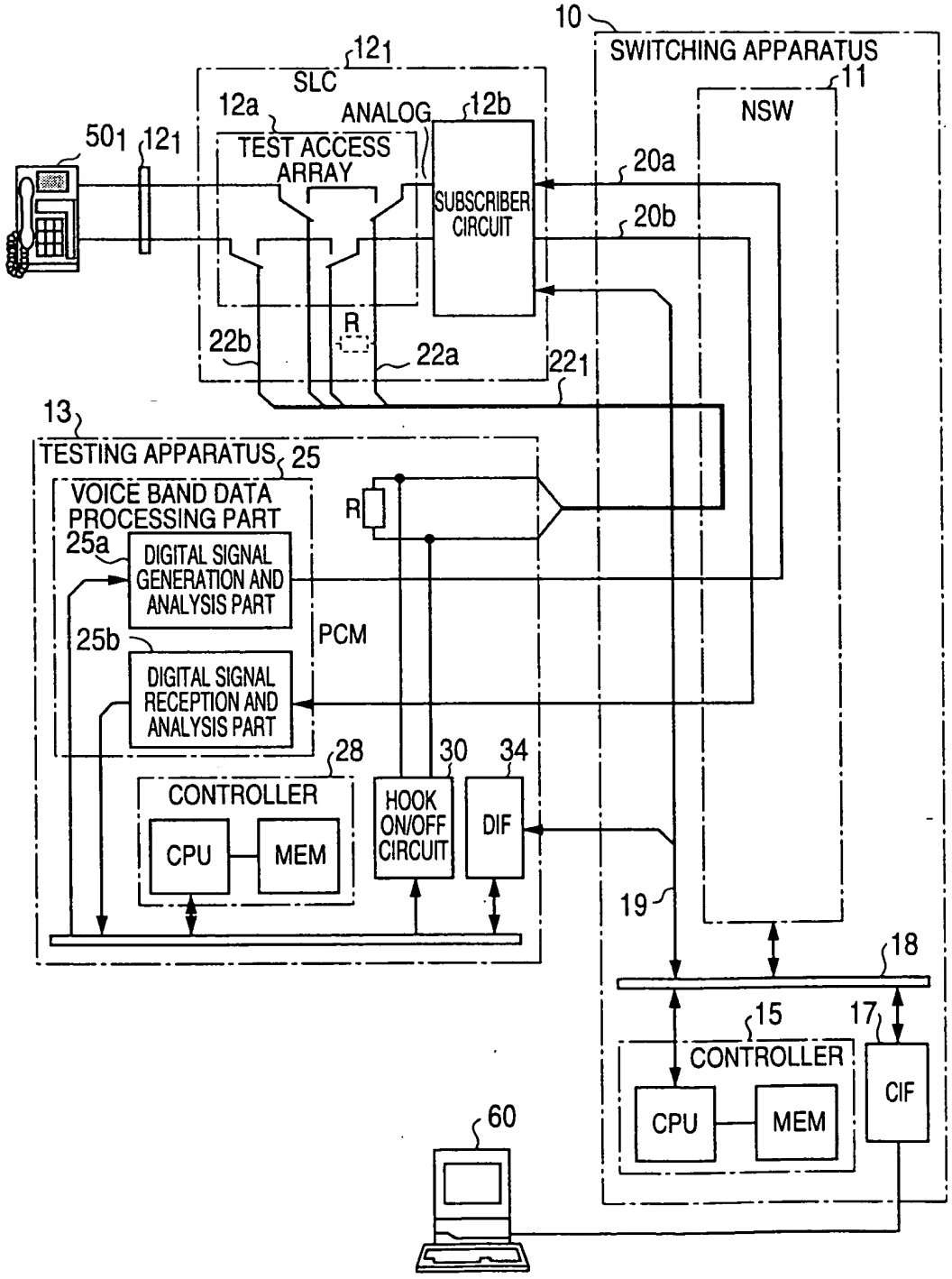

10
SWITCHING APPARATUS
11
NSW
121
SLC
12a
ANALOG
TEST ACCESS ARRAY
12b
SUBSCRIBER CIRCUIT
501
121
20a
20b
R
22b
22a
221
13
TESTING APPARATUS
25
VOICE BAND DATA PROCESSING PART
25a
DIGITAL SIGNAL GENERATION AND ANALYSIS PART
PCM
25b
DIGITAL SIGNAL RECEPTION AND ANALYSIS PART
28
CONTROLLER
CPU
MEM
30
HOOK ON/OFF CIRCUIT
34
DIF
19
18
15
17
CONTROLLER
CPU
MEM
CIF
60

FIG. 14

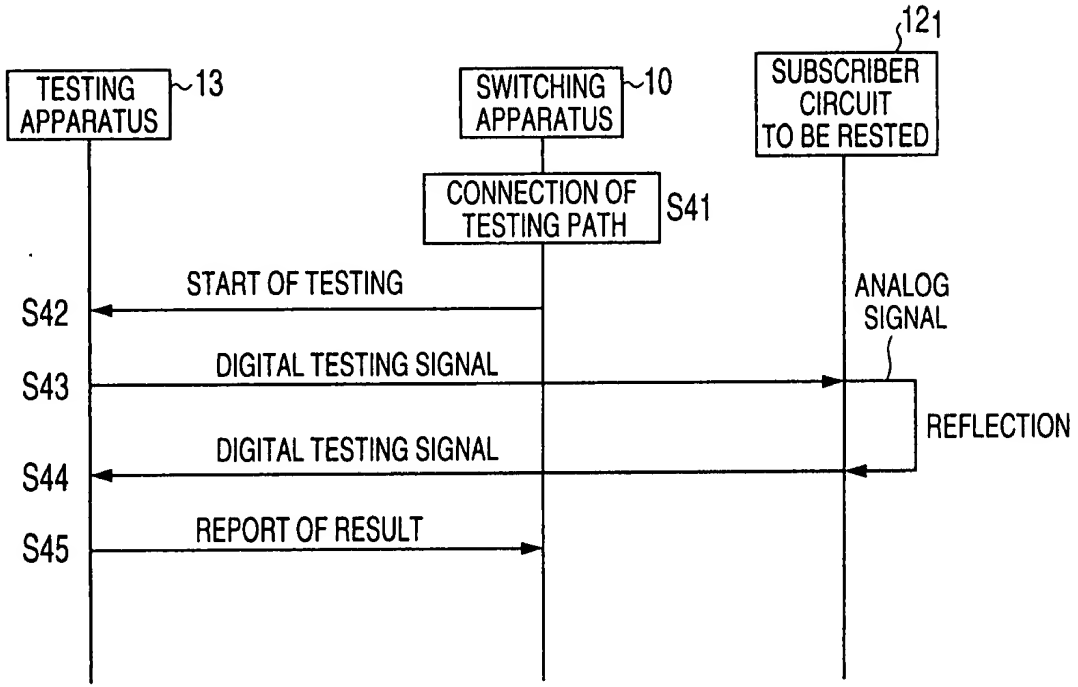

TESTING APPARATUS
13
SWITCHING APPARATUS
10
SUBSCRIBER CIRCUIT TO BE RESTED
121
CONNECTION OF TESTING PATH
S41
START OF TESTING
S42
ANALOG SIGNAL
DIGITAL TESTING SIGNAL
S43
REFLECTION
DIGITAL TESTING SIGNAL
S44
REPORT OF RESULT
S45

FIG. 15

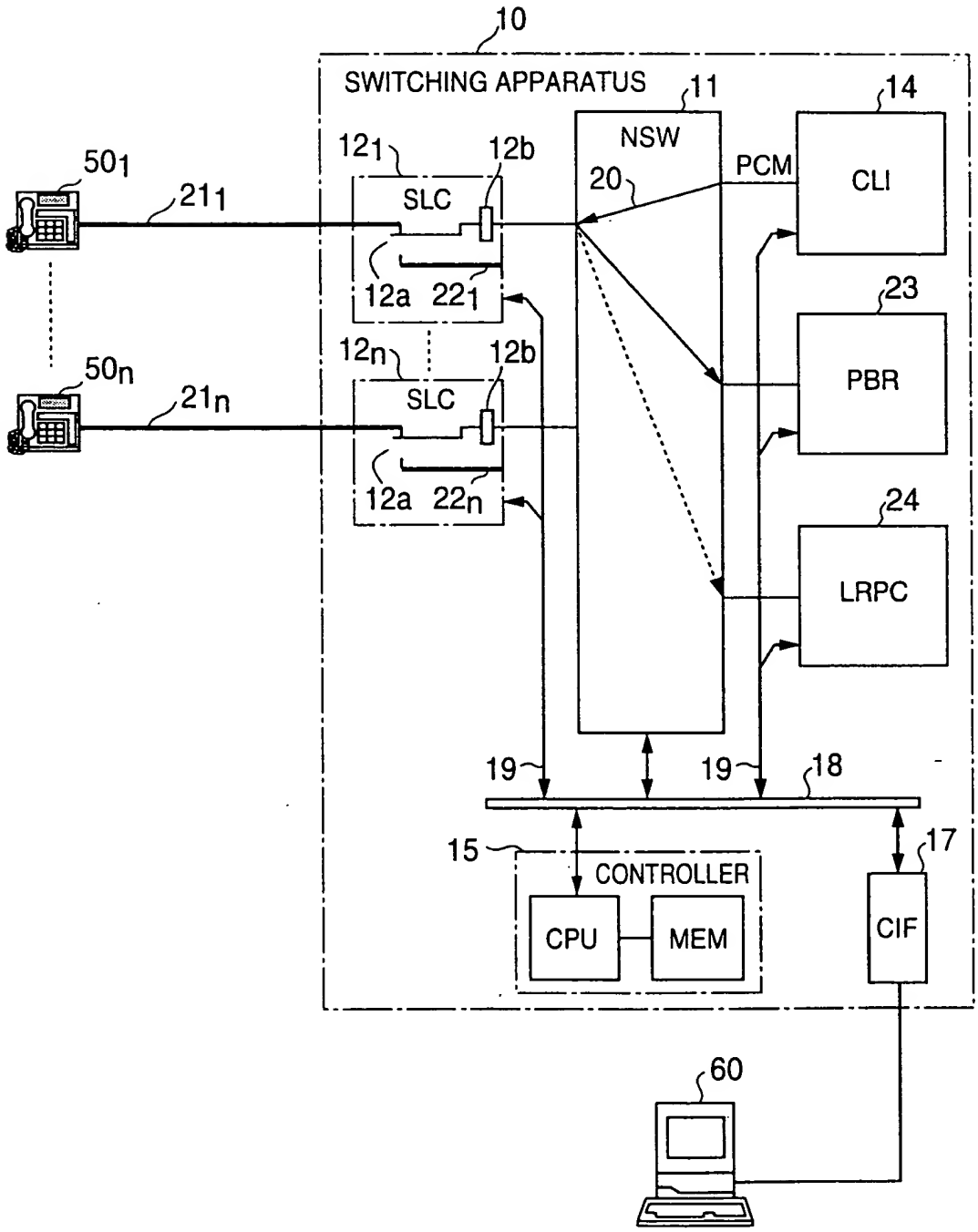

10
SWITCHING APPARATUS
11
NSW
14
CLI
PCM
20
121
12b
SLC
501
211
12a
221
12n
22n
50n
21n
23
PBR
24
LRPC
19
18
15
CONTROLLER
CPU
MEM
17
CIF
60

FIG. 16

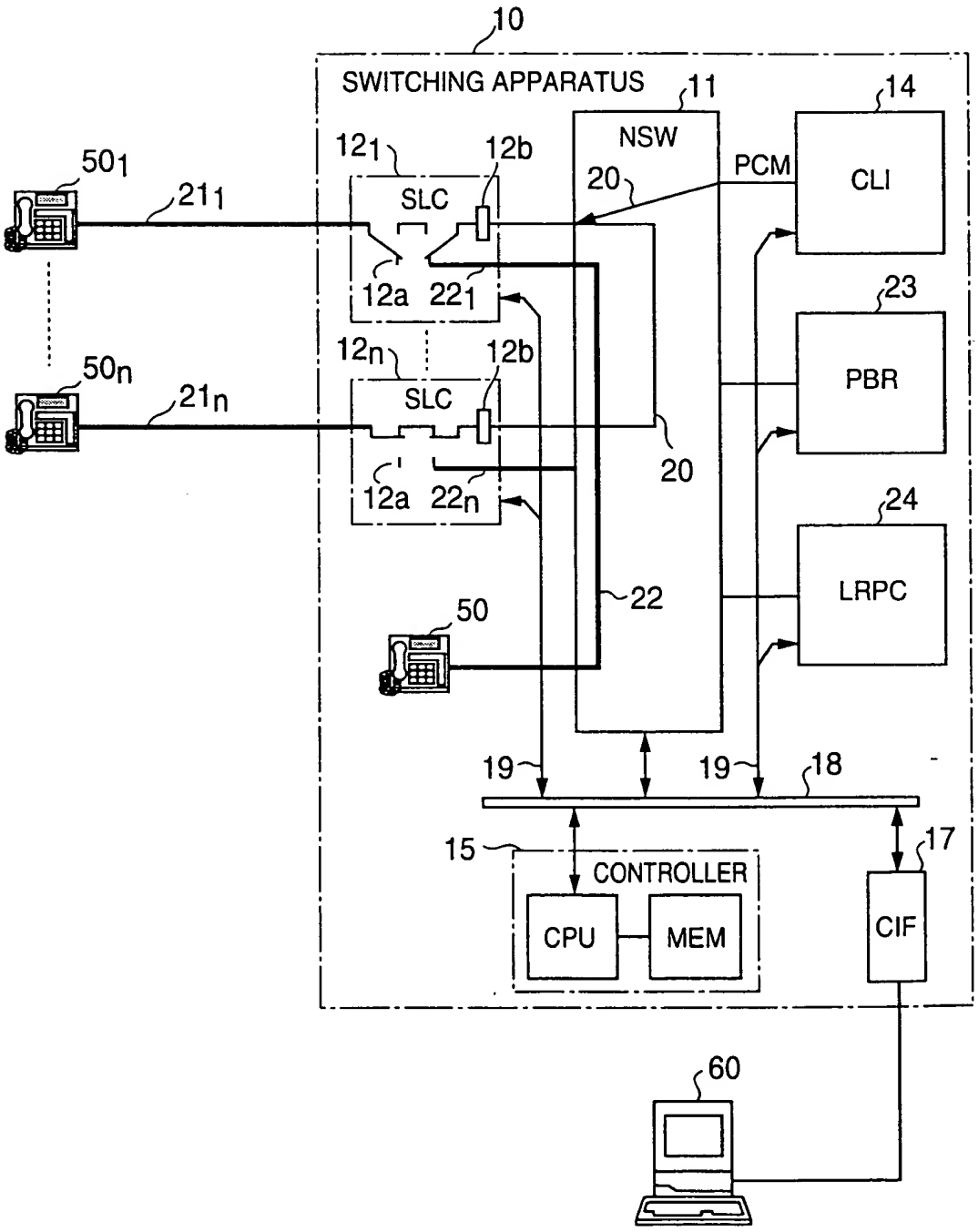
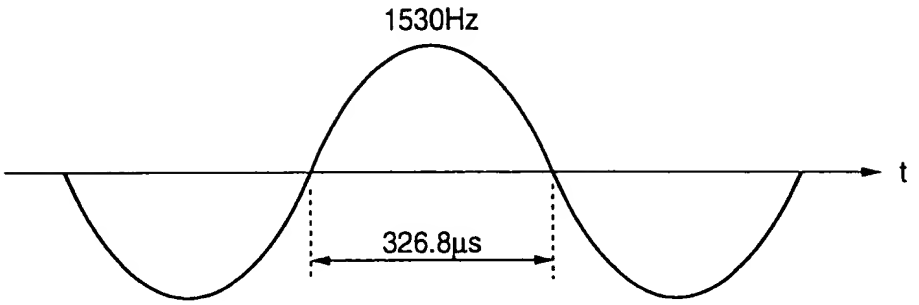
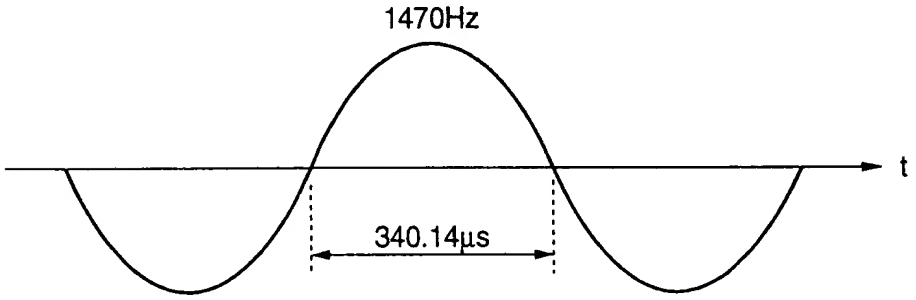

10
SWITCHING APPARATUS
11
NSW
14
CLI
PCM
20
121
12b
SLC
501
211
12a
221
12n
50n
21n
22n
23
PBR
24
LRPC
22
50
19
18
17
15
CONTROLLER
CPU
MEM
CIF
60

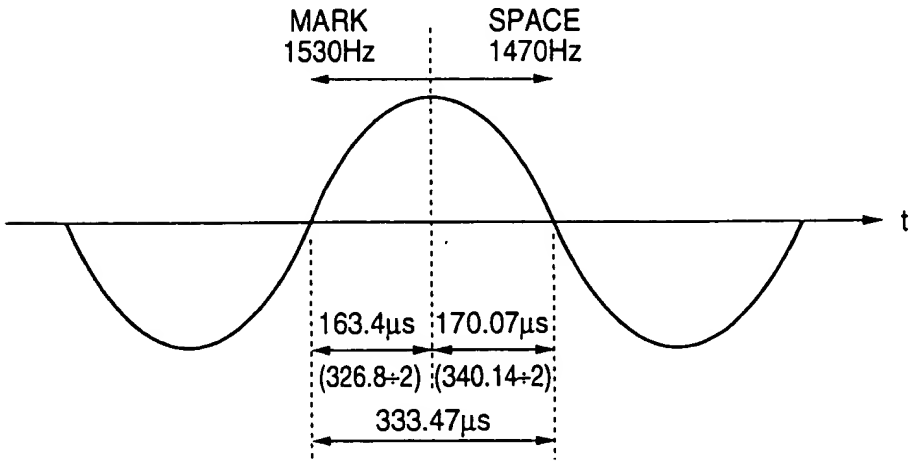
FIG. 17



(A) MARK



(B) SPACE



(C) MARK / SPACE

FIG. 18

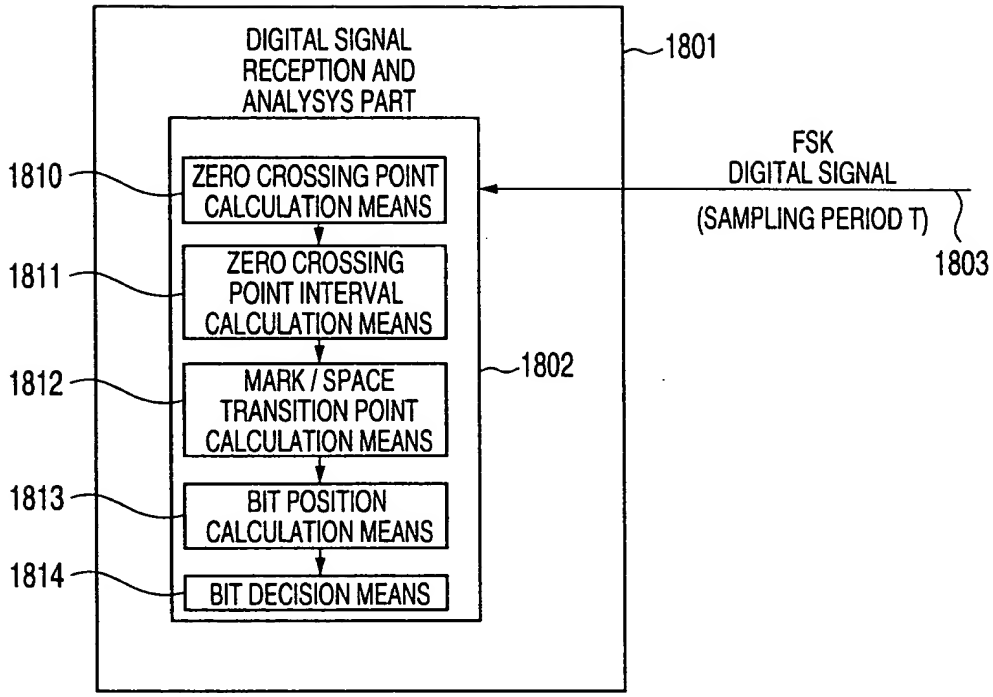

DIGITAL SIGNAL RECEPTION AND ANALYSYS PART
1801
1810
ZERO CROSSING POINT CALCULATION MEANS
1811
ZERO CROSSING POINT INTERVAL CALCULATION MEANS
1812
MARK / SPACE TRANSITION POINT CALCULATION MEANS
1813
BIT POSITION CALCULATION MEANS
1814
BIT DECISION MEANS
1802
FSK DIGITAL SIGNAL
(SAMPLING PERIOD T)
1803

FIG. 19

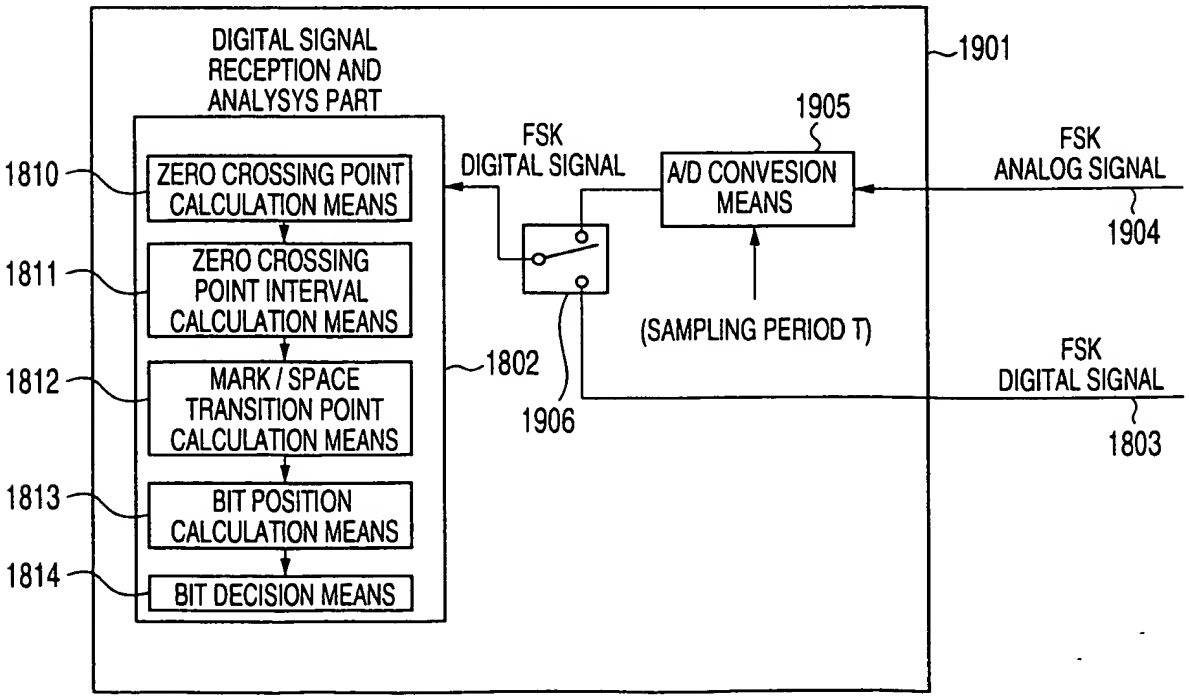

DIGITAL SIGNAL RECEPTION AND ANALYSYS PART
1901
1905
FSK DIGITAL SIGNAL
A/D CONVESION MEANS
FSK ANALOG SIGNAL
1904
1810
ZERO CROSSING POINT CALCULATION MEANS
1811
ZERO CROSSING POINT INTERVAL CALCULATION MEANS
1812
MARK / SPACE TRANSITION POINT CALCULATION MEANS
1813
BIT POSITION CALCULATION MEANS
1814
BIT DECISION MEANS
1802
(SAMPLING PERIOD T)
FSK DIGITAL SIGNAL
1906
1803

FIG. 20

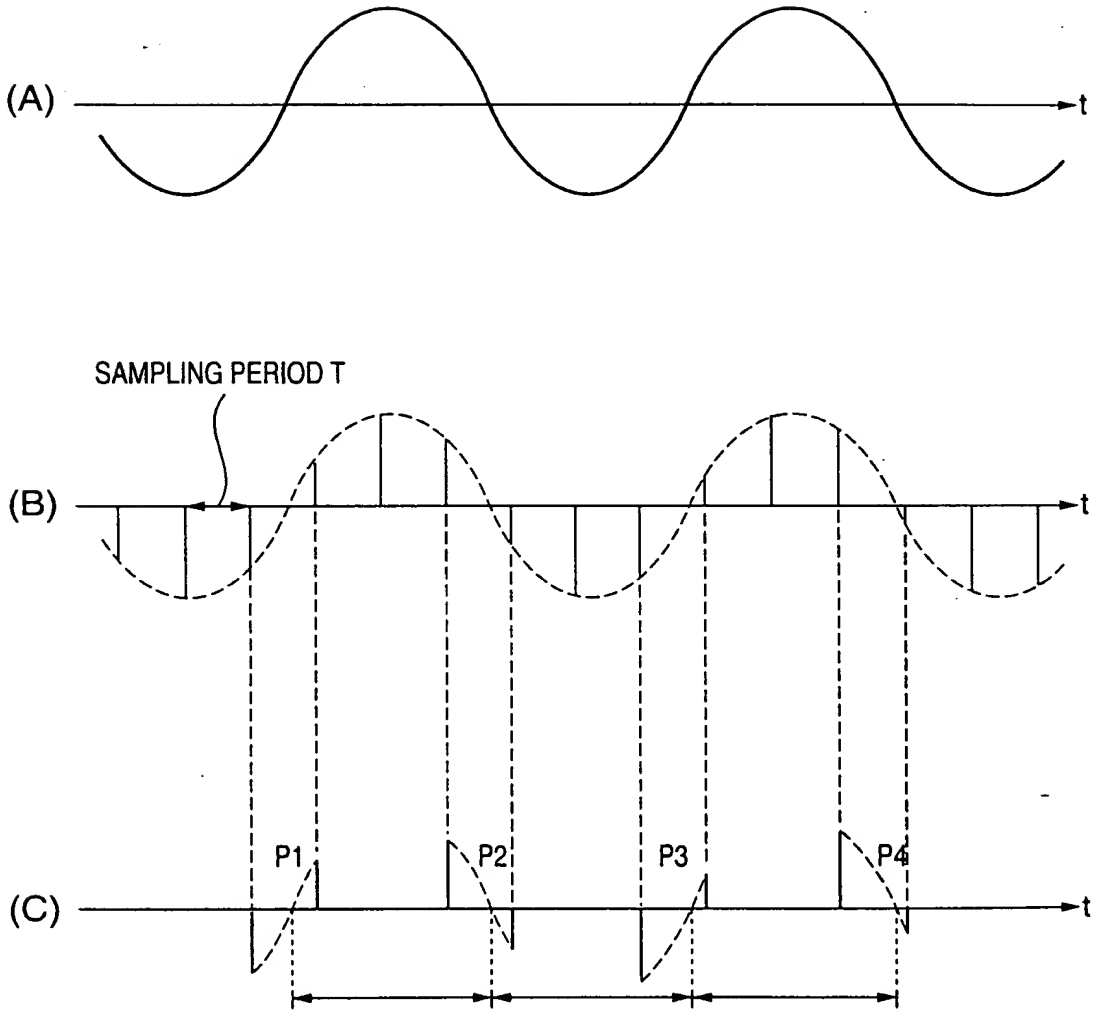


FIG. 21

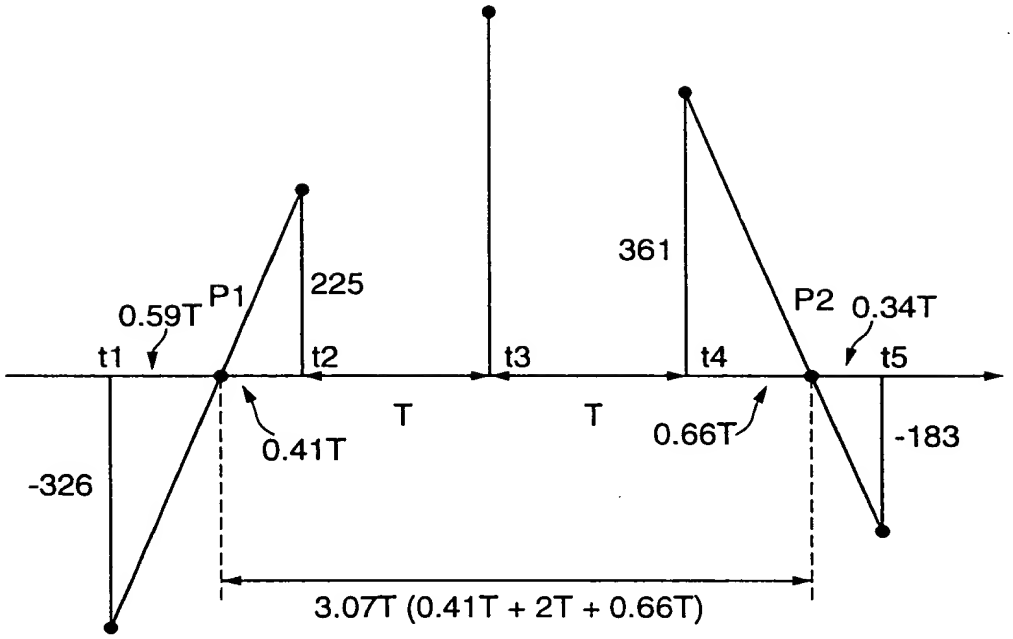
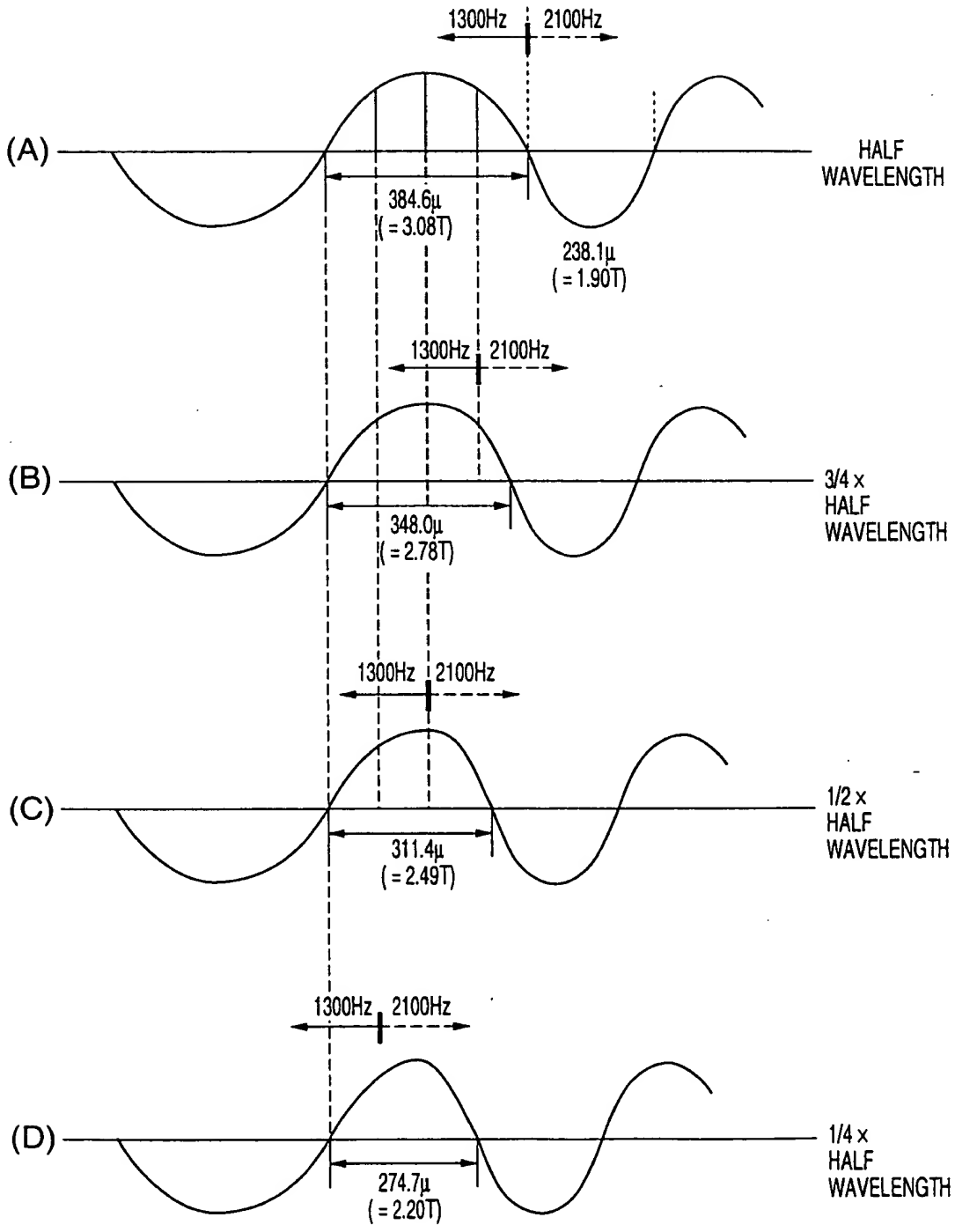

0.59T
P1
225
361
P2
0.34T
t1
t2
t3
t4
t5
T
T
0.41T
0.66T
-326
-183
3.07T (0.41T + 2T + 0.66T)

FIG. 22


1300Hz
2100Hz
(A)
HALF WAVELENGTH
384.6μ (= 3.08T)
238.1μ (= 1.90T)
1300Hz
2100Hz
(B)
3/4 x HALF WAVELENGTH
348.0μ (= 2.78T)
1300Hz
2100Hz
(C)
1/2 x HALF WAVELENGTH
311.4μ (= 2.49T)
1300Hz
2100Hz
(D)
1/4 x HALF WAVELENGTH
274.7μ (= 2.20T)

D05007 "82682960

FIG. 23

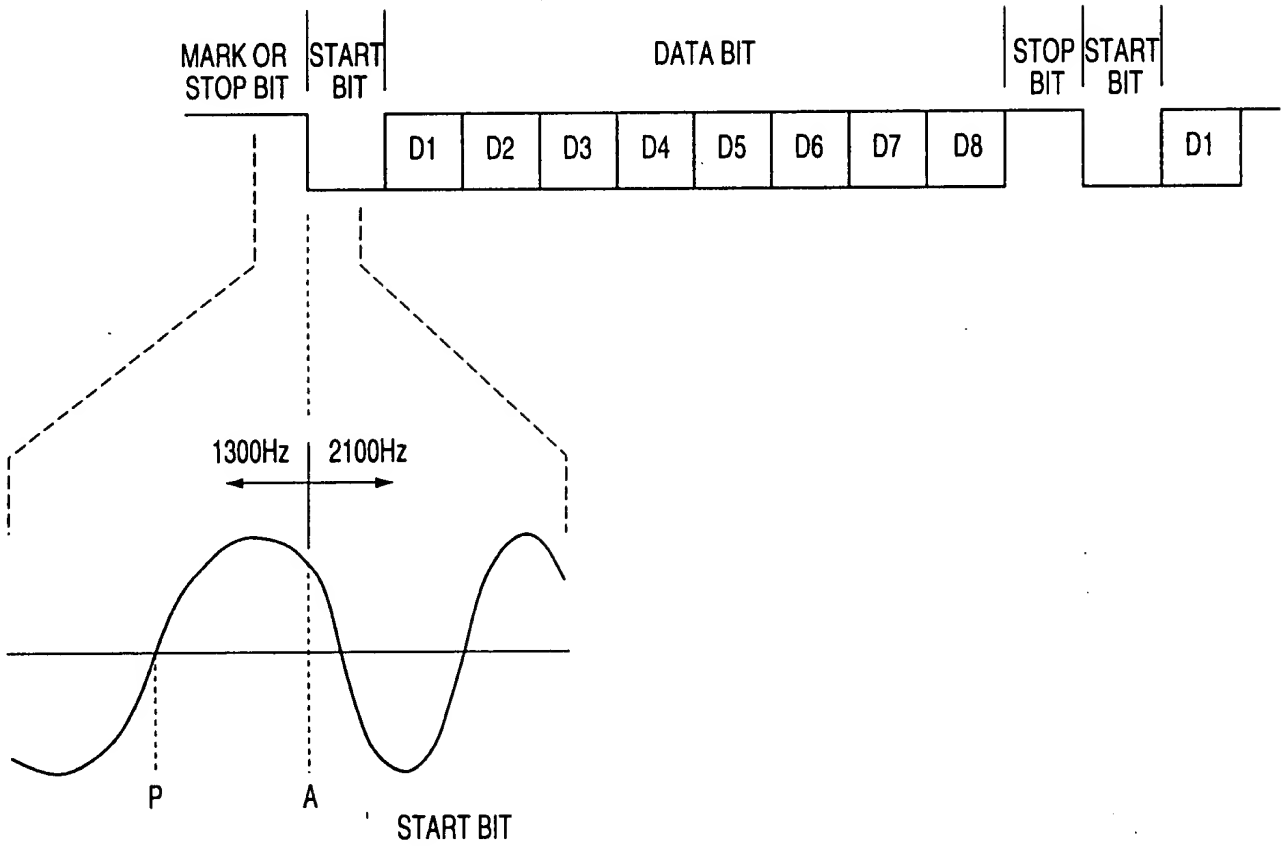


FIG. 24

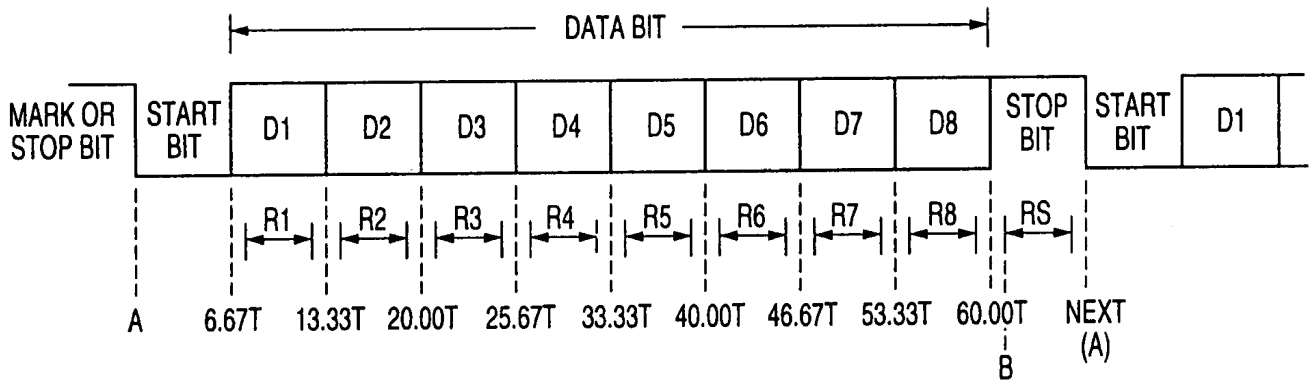
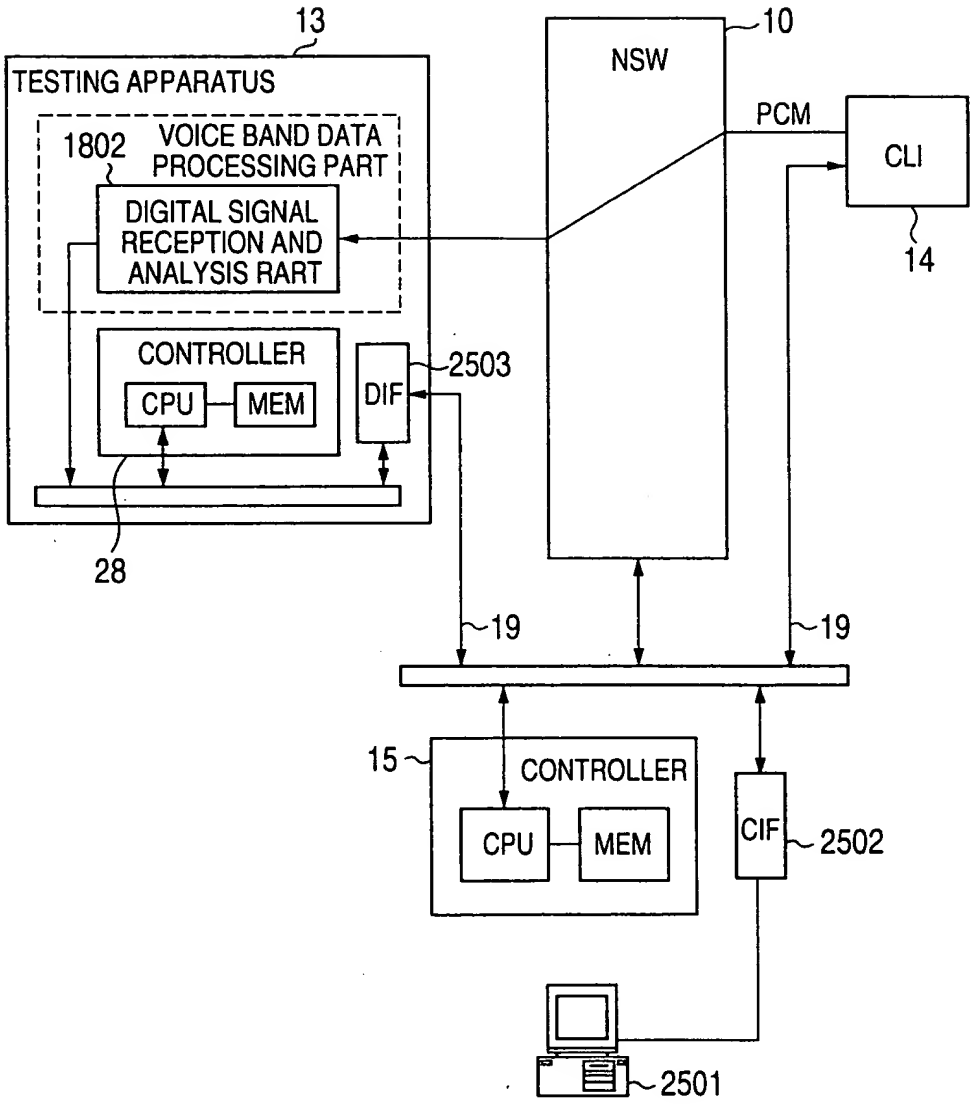

DATA BIT
MARK OR STOP BIT
START BIT
D1
D2
D3
D4
D5
D6
D7
D8
STOP BIT
START BIT
D1
R1
R2
R3
R4
R5
R6
R7
R8
RS
A
6.67T
13.33T
20.00T
25.67T
33.33T
40.00T
46.67T
53.33T
60.00T
B
NEXT (A)

FIG. 25


13
TESTING APPARATUS
1802
VOICE BAND DATA PROCESSING PART
DIGITAL SIGNAL RECEPTION AND ANALYSIS RART
CONTROLLER
CPU
MEM
DIF
2503
28
NSW
10
PCM
CLI
14
19
19
15
CONTROLLER
CPU
MEM
CIF
2502
2501